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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,451	12/05/2003	Roy E. Scheuerlein	MA-112	9337

7590 10/06/2005

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EXAMINER	
RICHARDS, N DREW	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 10/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/728,451	SCHEUERLEIN ET AL.	
	Examiner	Art Unit	
	N. Drew Richards	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-94* is/are pending in the application.

4a) Of the above claim(s) *16-26,44-54,70-72 and 75-80* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15,27-43,55-69,73,74 and 81-94* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/8/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I and Species IA in the reply filed on 7/15/05 is acknowledged. Applicant has indicated that claims 1-15, 27-43, 55-69 and 73 read on the elected invention. These claims, as well as linking claims 74 and 81-94 are examiner herein.

Information Disclosure Statement

2. The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609.04(a) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

Specification

3. The disclosure is objected to because of the following informalities: the first line of paragraph [0001] is objected to since applicant has not provided the application serial number for the related application.

Appropriate correction is required.

Drawings

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the fourth pitch substantially less than or substantially one half of the first pitch (as recited in claims 28, 29, 43, 69 and 85) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 1 recites the limitation "the substrate" in line 11. There is insufficient antecedent basis for this limitation in the claim.

7. Claim 15 recites the limitation "the memory lines" in line 1. There is insufficient antecedent basis for this limitation in the claim.

8. Claim 30 recites the limitation "the substrate" in line 13. There is insufficient antecedent basis for this limitation in the claim.

9. Claim 56 recites the limitation "the substrate" in line 12. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 1-6, 30-34, 56-60, 74, 81-84 and 94 are rejected under 35 U.S.C. 102(b) as being anticipated by Iwasaki (US Patent No. 6,034,436).

With regard to claim 1, Iwasaki disclose in figure 7B a structure for providing multilevel electrical connectivity within an integrated circuit (note that figure 7B shows a portion of a cross section that will repeat many times on the chip), the structure comprising:

- a first plurality of vias D1/D3;
- a second plurality of vias D2, wherein the first and second pluralities of vias are vertically overlapping;
- a first routing level S2 at a first height, the first level connected to the first plurality of vias; and
- a second routing level S1 at a second height connected to the second plurality of vias, wherein the first height is different from the second height;
- where both routing levels are formed above the substrate, and the first and second routing levels are below the first and second vias.

With regard to claim 2, the first and second vias are evenly spaced and have a first common pitch.

With regard to claim 3, the first routing level has a second pitch and the second routing level has a third pitch, the first pitch smaller than the second and third pitch.

With regard to claims 4 and 5, a third routing level U1/U2/U3 is above the vias opposite the first and second routing levels.

With regard to claim 6, the third routing levels are memory lines. Iwasaki discloses an improved through hole structure and teaches that through hole/interconnect structures are used for memory arrays.

With regard to claim 30, Iwasaki anticipates this claim in a manner similar to claims 1 and 4 above.

With regard to claim 31, the first and second vias are evenly spaced and have a first common pitch.

With regard to claim 32, the third routing level U1/U2/U3 is above the first and second routing levels.

With regard to claim 33, the third routing levels are memory lines. Iwasaki discloses an improved through hole structure and teaches that through hole/interconnect structures are used for memory arrays.

With regard to claim 34, the first routing level has a second pitch and the second routing level has a third pitch, the first pitch smaller than the second and third pitch.

With regard to claims 56-60, these claims are anticipated in a manner similar to claims 1-6 above.

With regard to claim 74, Iwasaki disclose a method for forming the device as claimed including forming the first and second routing levels with the second routing level above the first, and forming first and second pluralities of vias connected at bottom ends to the routing levels, wherein the first and second pluralities of vias are vertically overlapping.

With regard to claims 81-84 and 94, these claims are rejected similarly to claims 2-6 above

12. Claims 1, 2, 4-7, 15, 28-33, 35, 43; 56-59, 69, 74, 81-83, 85, 86 and 94 are rejected under 35 U.S.C. 102(b) as being anticipated by Amanuma (US 2001/0038115 A1).

Amanuma discloses a device as claimed in figure 2, for example. The cross section in figure 2 shows a portion of the repeating structure of an array, thus this cross section is repeated many times. With regard to claim 1, Amanuma discloses:

- a first plurality of vias (12 on the right side of the transistors formed below);
- a second plurality of vias (12 on the left side of the transistors formed below);
- a first routing level at a first height (10) connected to the first plurality of vias;
- a second routing level at a second height (7) connected to the second plurality of vias, where the first height is different from the second height;
- where both routing levels are formed above the substrate 1 and the first and second routing levels are below the vias.

With regard to claim 2, the first and second vias are evenly spaced and have a first common pitch.

With regard to claims 4 and 5, Amanuma disclose a third routing level 18 above the first and second vias vertically opposite the first and second routing levels.

With regard to claims 6 and 7, the third routing level comprises memory lines in a memory array where cells accessed by the memory lines are charge storage cells (capacitors).

With regard to claims 15, 28 and 29, the memory lines have a fourth pitch smaller than the first pitch, further wherein the fourth pitch is substantially one half the first pitch.

With regard to claim 30, Amanuma anticipates this claim in a manner similar to claims 1 and 4 above.

With regard to claim 31, the first and second vias are evenly spaced and have a first common pitch.

With regard to claim 32, the third routing level 18 is above the first and second routing levels.

With regard to claim 33, the third routing levels are memory lines.

With regard to claim 35, the third routing level comprises memory lines in a memory array where cells accessed by the memory lines are charge storage cells (capacitors).

With regard to claim 43, the memory lines have a fourth pitch smaller than the first pitch.

With regard to claims 56-59, these claims are anticipated in a manner similar to claims 1, 2 and 4 above.

With regard to claim 69, the memory lines have a fourth pitch smaller than the first pitch.

With regard to claim 74, Amanuma discloses a method for forming the device as claimed including forming the first and second routing levels with the second routing level above the first, and forming first and second pluralities of vias connected at bottom ends to the routing levels, wherein the first and second pluralities of vias are vertically overlapping.

With regard to claims 81-83 and 94, these claims are rejected similarly to claims 2, 4 and 5 above

With regard to claim 85, the memory lines have a third pitch smaller than the first pitch.

With regard to claim 86, the third routing level comprises memory lines in a memory array where cells accessed by the memory lines are charge storage cells (capacitors).

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 7-14, 27, 35-42, 55, 61-68, 73 and 86-93 rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki as applied to claims 1-6, 30-34, 56-60, 74, 81-84 and 94 above.

Iwasaki teach the structure of the interconnections with first, second and third routing levels and first and second pluralities of vias. However, Iwasaki does not teach the particular device that the interconnects are used to connect. Thus, Iwasaki does not explicitly teach the memory cells being charge storage memory cells, SONOS devices, floating gate devices, arranged in a NAND string, passive element memory cells including a fuse or antifuse, of a monolithic three dimensional memory array which further comprises at least first and second memory levels with the second memory level formed above the first. Though not explicitly taught by the reference, it is considered

nonetheless obvious to one of ordinary skill in the art to employ the improved through-hole structure of Iwasaki to any known memory device structure and array. There is nothing inventive in using a known through-hole structure for semiconductor devices in any of the claimed variety of memory cells and arrays. One of ordinary skill in the art would have found it obvious to combine the through-hole layout of Iwasaki into the known memory arrays and structures in order to reduce the occupied area for the interconnections.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Keeth (US Patent No. 6429529 B1), Park et al. (US Patent No. 6822330 B2).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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